REMARKS

In the Final Office Action of October 19, 2007, the Examiner: (1) rejected claims 1-4, 6-10, 12-16 and 18-26 as allegedly obvious over Eggleston (U.S. Patent No. 6,906,961) in view of Wei (U.S. Patent No. 6,683,817); and (2) rejected claims 5, 11 and 17 as allegedly obvious over Eggleston in view of Kikuchi (U.S. Patent No. 6,594,792) further in view of Acton (6,883, 131);

With this response, Applicant amends claims 1, 3-4, 6, 10, 12, 14, 16 and 18-19. Applicant believes that the pending claims are allowable over the art of record and respectfully request reconsideration.

I. ART BASED REJECTIONS

A. Claim 1

Claim 1 stands rejected as allegedly obvious over Eggleston and Wei. Applicant amends claim 1 to define over Wei's teaching of generating ECC while writing data between a SRAM and a NAND flash.

Eggleston is directed towards erase block data splitting. (Eggleston Title). In particular, Eggleston teaches flash memory devices that splits the user data from the associated overheard data among separate flash memory devices to avoid the issue of potential corruption. (Eggleston Col. 2, lines 60-67). Eggleston teaches that a flash memory physical sector contains four 512 bytes logical sectors and four ECC code areas. (Eggleston Col. 13, lines 14-42). Further, Eggleston teaches that ECC hardware generates the required ECC for the user data written into the logic sectors of the current write accessed physical sector and stores the ECC in a RAM storage circuit. (Eggleston Col. 16, lines 31-48). When the next physical sector is writes accessed, the ECC from the RAM storage circuit is written out to the ECC code area of the next physical sector. (Eggleston Col. 16, lines 31-48).

Claim 1, by contrast, specifically recites "computing an ECC for said data block while transferring the data block; and selectively storing the ECC in a plurality of registers using a switching mechanism." Applicant submits that Eggleston and Wei fail to teach or fairly suggest such a method. In particular, Eggleston appears to teach storing the ECC in RAM storage, and then writing it out to the ECC code area of the flash memory, but is silent to storing the ECC using a switching mechanism in a plurality of registers.

Thus, even if the teachings of Wei are precisely as the Office Action suggested (which the Applicant does not admit), Eggleston and Wei still fail to teach or fairly suggest "computing an ECC for said data block while transferring the data block; and **selectively storing the ECC in a plurality of registers using a switching mechanism**."

Based at least on the foregoing Applicant submits that claim 1 all claims which depend on claim 1 (claims 2-5) should be allowed. Applicants amend claims 3-4 to be consistent with claim 1 and not to define over any of the cited art.

B. Claim 6

Claim 6 stands rejected as allegedly obvious over Eggleston and Wei. Applicant amends claim 6 to define over Wei's teaching of generating ECC while writing data between a SRAM and a NAND flash.

Claim 6 specifically recites "said controller is configured to shift a data block between the flash memory and the controller while computing an ECC for said data block; and said system is configured to selectively store the ECC in a plurality of registers using the switch." Applicant submits that Eggleston and Wei fail to teach or fairly suggest such a method. In particular, Eggleston appears to teach storing the ECC in RAM storage, and then writing it out to the ECC code area of the flash memory, but is silent to storing the ECC using a switching mechanism in a plurality of registers. Thus, even if the teachings of Wei are precisely as the Office Action suggested (which the Applicant does not admit), Eggleston and Wei still fail to teach or fairly suggest "said controller is configured to shift a data block between the flash memory and the controller while computing an ECC for said data block; and **said system is configured to selectively store the ECC in a plurality of registers using the switch**."

Based at least on the foregoing Applicant submits that claim 8 all claims which depend on claim 8 (claims 9-11 and 24-26) should be allowed. Applicant amends dependent claims 10 to be consistent with claim 6, and not to define over any cited art.

C. Claim 12

Claim 12 stands rejected as allegedly obvious over Eggleston and Wei. Applicant amends claim 12 to define over Wei's teaching of generating ECC while writing data between a SRAM and a NAND flash.

Claim 12 specifically recites "a means for shifting the data block between the means for storing and the means for controlling while computing an ECC for said data block; and a means for selectively storing the ECC in a plurality of registers." Applicant submits that Eggleston and Wei fail to teach or fairly suggest such a method. In particular, Eggleston appears to teach storing the ECC in RAM storage, and then writing it out to the ECC code area of the flash memory, but is silent to storing the ECC using a switching mechanism in a plurality of registers. Thus, even if the teachings of Wei are precisely as the Office Action suggested (which the Applicant does not admit), Eggleston and Wei still fail to teach or fairly suggest "a means for shifting the data block between the means for storing and the means for controlling while computing an ECC for said data block; and **a means for selectively storing the ECC in a plurality of registers**."

Based at least on the foregoing Applicant submits that claim 12 all claims which depend on claim 12 (claims 13-17) should be allowed. Applicant amends dependent claims 14 and 16 to be consistent with claim 12, and not to define over any cited art.

D. Claim 18

Claim 18 stands rejected as allegedly obvious over Eggleston and Wei. Applicant amends claim 18 to define over Wei's teaching of generating ECC while writing data between a SRAM and a NAND flash.

Claim 18 specifically recites "an ECC engine configured to compute an ECC while transferring a data block between the ECC engine and memory; and a switching mechanism coupled to the ECC engine, the ECC engine configured to selectively store the ECC in a plurality of registers using the switching mechanism." Applicant submits that Eggleston and Wei fail to teach or fairly suggest such a method. In particular, Eggleston appears to teach storing the ECC in RAM storage, and then writing it out to the ECC code area of the flash memory, but is silent to storing the ECC using a switching mechanism in a plurality of registers. Thus, even if the teachings of Wei are precisely as the Office Action suggested (which the Applicant does not admit), Eggleston and Wei still fail to teach or fairly suggest "an ECC engine configured to compute an ECC while transferring a data block between the ECC engine and memory; and **a switching mechanism coupled to the ECC engine, the ECC engine configured to selectively store the ECC in a plurality of registers using the switching mechanism**."

Based at least on the foregoing Applicant submits that claim 18 all claims which depend on claim 18 (claims 19-23) should be allowed. Applicant amends dependent claim 19 to be consistent with claim 18, and not to define over any cited art.

II. CONCLUSION

In course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. If the Examiner feels that a telephone conference would expedite the resolution of this case, he is respectfully requested to contact the undersigned. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to the Texas Instruments, Inc. Deposit Account No. 20-0668.

Respectfully submitted,

/Utpal D. Shah/

Utpal D. Shah
PTO Reg. No. 60,047
CONLEY ROSE, P.C.
(512) 391-1900 (Phone)
(512) 320-9181 (Fax)
AGENT FOR APPLICANTS